



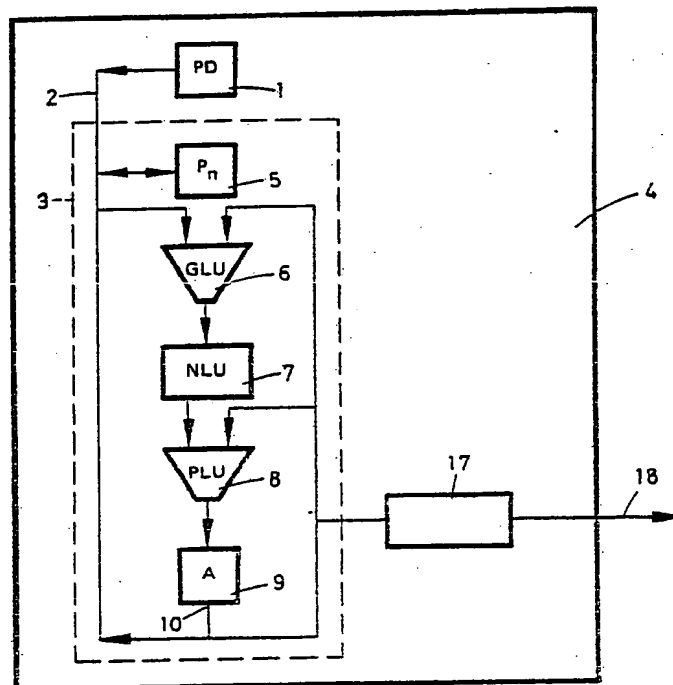
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(54) Title: DEVICE FOR AN ARRAY OF PHOTO DIODES ARRANGED IN A MATRIX

(57) Abstract

A device for an array (1) of photo diodes arranged in a matrix, which are integrated onto the same semi-conductor substrate (4) as a picture processor (3) connected to the photo diodes. The picture processor (3) is of a type allowing parallel signal processing, such as a picture transformation of the picture signals coming from the photo diodes. The characteristic of the invention is that the device includes a digital circuit (17) of combinatorial or sequential type connected to the processor (3). This is arranged on said substrate and designed to determine the number and/or the position and/or the sum of positions of the picture elements which the photo diodes (1) and the picture processor (3) have established to fulfil a digital criterion.



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Device for an array of photo diodes arranged in a matrix

The present invention relates to a device for an array of photo diodes arranged in a matrix, which are integrated to the same semi-conductor substrate as a picture processor connected to the photo diodes, where the picture processor is of a type allowing parallel signal processing, such as picture transformation of the picture signals coming from the photo diodes.

Computerized picture processing had already been introduced in the sixties but it is only during recent years that it has become industrially interesting as equipment and algorithms have reached a sufficient level of maturity. This kind of picture processing has so far been realized in discrete systems where a TV camera and a computer have been the basic components.

To reach a more efficient usage of this technique the inventors at the Tenth Nordic Semi-conductor Convention, June 1982, have suggested an integrated solution including a camera in the form of a photo diode matrix as well as a picture processor. Such a picture processor is characterized by a high parallelism and therefore performs rapid operations on pictures.

This kind of system has so far only been implemented as prototypes. When using these it has become obvious that the efficiency which is desired by the integration is jeopardized because the picture processing result cannot be extracted rapidly and efficiently from the circuit. One of the drawbacks is that a resulting picture must be read out from the circuit as this picture generally is the base for following, numerical calculations. As the number of connections to the circuit is considerably less than the number of picture elements this read out must take place serially which eliminates some of the speed advantage of the fast picture processor.

This invention aims to cure this disadvantage and this is achieved in that the device includes a digital circuit of a combinatorial or sequential type connected to the processor and designed to determine the number and/or the position of the picture elements which the photo diodes and the picture processor have established to fulfil a digital criterion.

The invention reduces the need to read out picture data by providing highly



compressed information which can be brought out easily and be used for further processing.

5 In the following the invention will be explained further referring to the enclosed drawing where fig 1 shows a block chart of a device according to the invention integrated onto a single semi-conductor substrate. Fig 2 shows a preferred embodiment of a digital circuit according to a special characteristic of the invention. Fig 3 shows a preferred embodiment of a circuit block included in the invention.

10 In fig 1, 1 represents a diode matrix consisting of a number of photo diodes (PD), which via a data bus 2 is connected to a picture processor 3 with as many channels as the number of photo diodes in the matrix. Although it is not clearly spelt out, it is obvious that all signals are transformed into digital form to be
15 able to be received and processed by the picture processor. The photo diode matrix 1 and the picture processor 3 are arranged on a common semi-conductor substrate using established semi-conductor technology and the picture processor is of the previously said type and capable of performing parallel picture processing operations.

20 Such a picture processor 3 includes an array of picture registers (P_n) 5, a global logical unit (GLU) 6, a neighbourhood logical unit (NLU) 7, a point logical unit (PLU) 8, and an accumulator register (A) 9. The picture registers 5 are communicating via the bus 2 with one of the inputs of the GLU 6 and with the
25 output 10 of the accumulator register 9. Said output is also connected to the other input of the GLU 6 and to one input of the PLU 8. The output of the GLU 6 is connected to the input of the NLU 7 and the output of this unit is connected to the other input of the PLU 8. The output of the PLU 8 is in turn connected to the input of the accumulator register. The GLU 6 is arranged to mark out such
30 objects of a picture delivered from the accumulator register 9, which are pointed to by a picture D coming from the data bus 2, where the picture in turn can originate from either the diode matrix 1 or the picture register array 5. To point to an object means that one states that at least one picture element in the picture A belongs to the object which will be marked out and therefore has a
35 certain binary value. Using picture D to point to an object means that a corresponding picture element is given said binary value.

A preferred design of the GLU 6 is shown in fig 3. For each photo diode in the



diode matrix 1 the GLU 6 includes a circuit block 11 each consisting of two AND-gates 12, 13 and the OR-gates 14, 15 and 16 each having two inputs. One input of the AND-gates 12, 13 is connected to the accumulator register 9, while the other input is connected to the respective output of the OR-gates 14, 15 respectively. The output of the AND-gates are connected to both inputs of the OR-gate 16. One input of the OR-gates 14, 15 is connected to the data bus 2. The other input of the OR-gate 14 is connected to the output of the AND-gate 12 in the neighbouring GLU circuit block on one side while the other input of the OR-gate 15 is connected with the output of the AND-gate 13 in the neighbouring GLU circuit block on the other side.

The circuit block 11 works as follows: If a corresponding picture element belongs to an object, i.e. $A=1$ there is a possibility that the picture element will be marked out i.e. $G=1$. The condition for the picture element to be marked out is that at least one of the outputs of the gates 14, 15 is set to "one". This is the case either when the picture point is exactly the one pointed to i.e. $D=1$, or when the outputs of the gates 12 or 13 of the neighbouring GLU circuit blocks are set to "one" i.e. when the corresponding picture elements have been found to belong to the object.

The effect of this is that the circuit blocks 11 included in the GLU 6 co-operates mutually via the output signals from the gates 12 and 13. The output signal (L) of the gate 12 can be considered as going from circuit block to circuit block in one direction and the output signal of the gate 13 as going from circuit block to circuit block in the other direction.

The NLU 7 is arranged to compare each local area of a picture coming from the GLU 6 with a template. When the picture co-incides with the template this is marked with a logical "one". In all other places the picture gets the logical value "zero". The NLU 7 is therefore used to mark edges or isolated points, but can also be made to shift or invert the picture.

The PLU 8 is arranged to carry out distinct logical operations of the type AND, OR and EXCLUSIVE-OR between two pictures, from the accumulator register 9 and from the NLU 7 respectively. For example the EXCLUSIVE-OR operation is used to mark differences between said pictures.

The picture register array 5 and the accumulator register 9 is used for



intermediate storing of pictures.

- According to the invention the device includes a digital circuit 17 of a combinatorial or sequential type. The circuit 17 arranged on the substrate 4 is designed to determine the number and/or the position of the picture elements which via the diode matrix 1 and the picture processor 3 has been established to fulfil a digital criterion. In fig 1 for example the circuit 17 is connected to the output 10 of the accumulator register 9, but it is obvious that the circuit 17 alternatively can be connected to any point in the processor where pictures exist.
- On the output 18 of the circuit 17 which can be connected to a calculation unit, preferably a computer, a digital number is achieved, which can form the base for calculating a number of characteristics of an object, such as the position, length, perimeter, area and the position of the centre of gravity.
- The build-up of a preferred design of a digital circuit 17 according to the invention is shown in fig 2. The circuit includes a number of comparators 19 which is the same as the number of photo diodes in the matrix 1. In fig 2 said number is for example 8.
- At each output of the respective comparators a multiplier 20 with two inputs is connected. The digital circuit 17 also includes a digital adder 21, of which the inputs are connected to the outputs of the multipliers 20 and of which the output forms the output 18 of the circuit.
- Each comparator 19 is designed to give the value 1 on the output if a corresponding picture element coincides with an external condition, for example delivered from the before mentioned computer.
- To the other input of the respective multipliers, constant values 1, 2, 3 8 are used corresponding to the position of the respective photo diode picture point and the respective outputs of the multipliers then determines the position of the picture point when said criterion is fulfilled and is numerically zero otherwise. The adder 21 is designed to sum up all the values coming from the multipliers 20 and its output signal, which is a single resulting numerical value is a measurement of the number of and/or the sum of the positions for the picture elements which fulfils said criterion. The first case is achieved when the multipliers are by-passed so that the output signals of the comparators 19 directly reach the adder 21.



It is obvious that the invention cannot be considered to be limited to the embodiment shown on the drawing and described above, but within the scope of the invention it can be varied in many ways. This concerns particularly the design of the digital circuit 17 and the GLU 6, which by means of Boolean algebra can
5 be transformed with an unchanged function so that other gate combinations than those shown, are achieved.



Claims

1. Device for an array (1) of photo diodes arranged in a matrix, which are integrated onto the same semi-conductor substrate (4) as a picture processor (3) connected to the photo diodes, where the picture processor (3) is of a type allowing parallel signal processing, such as picture transformation of the picture signals coming from the photo diodes, characterized in that, the device includes a digital circuit (17) of a combinatorial or sequential type arranged on said substrate (4) and connected to the processor (3) and designed to determine the number and/or the position and/or the sum of the positions of the picture elements which the photo diodes (1) and the picture processor (3) have established to fulfil a digital criterion.
2. Device according to claim 1, characterized in that, said digital circuit (17) includes the same number of comparators (19) as there are photo diodes and where the comparators (19) are connected to the picture processor and arranged to generate the numerical digit "one" at the output with each picture element that corresponds to an external criterion, the same number of multipliers (20) as there are comparators (19) and where the multipliers (20) are connected to the respective comparator output and arranged to generate an output indicating the position of the picture point when said criterion is fulfilled and numerically "zero" otherwise, and a digital adder (21) where the inputs are connected to the outputs of the multipliers (20) and where the output is a measurement of the number and/or the position of the picture elements and/or the sum of the positions of the picture elements which fulfil said criterion.
3. Device according to claim 1 including circuit blocks (11), one for each photo diode, to mark picture points belonging to a connected object, characterized in that, each circuit block (11) is arranged to generate a binary signal corresponding to the object when the picture point belonging to it both fulfils a specific criterion for the object and at the same time has been selected as belonging to the object or when the picture points nearest to it has been marked out.



FIG 1

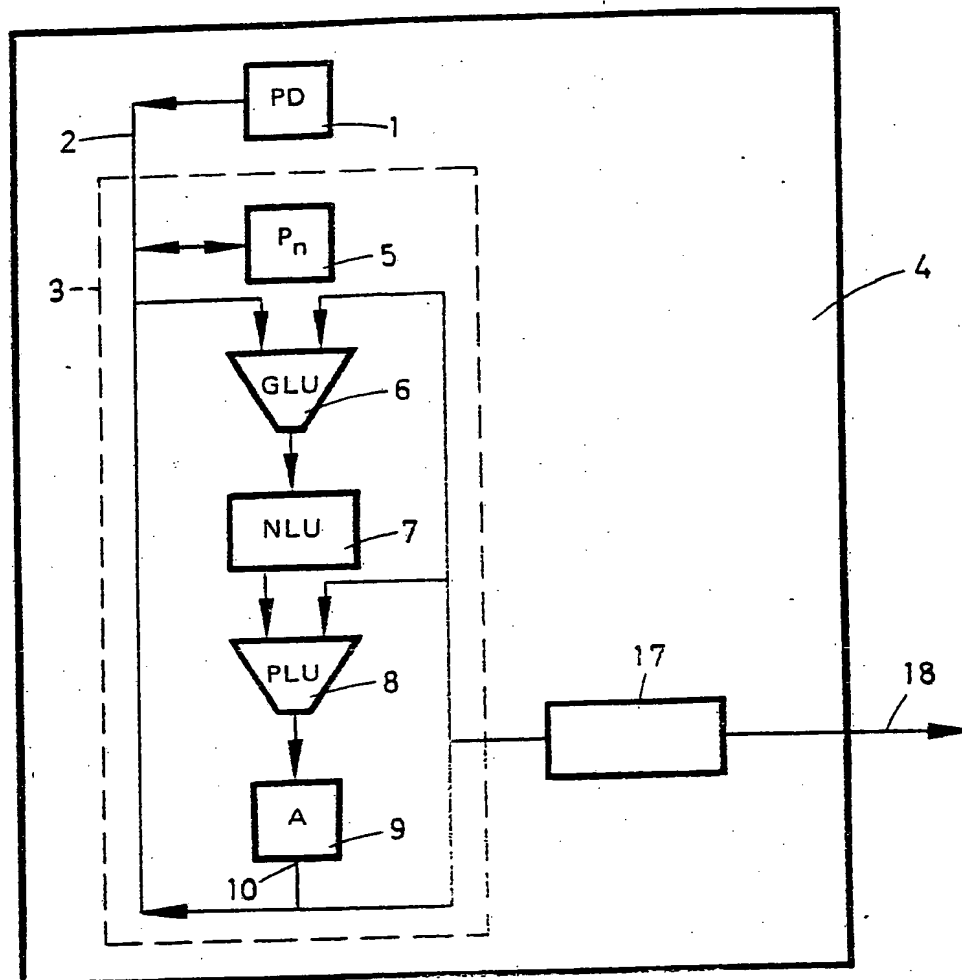


FIG 2

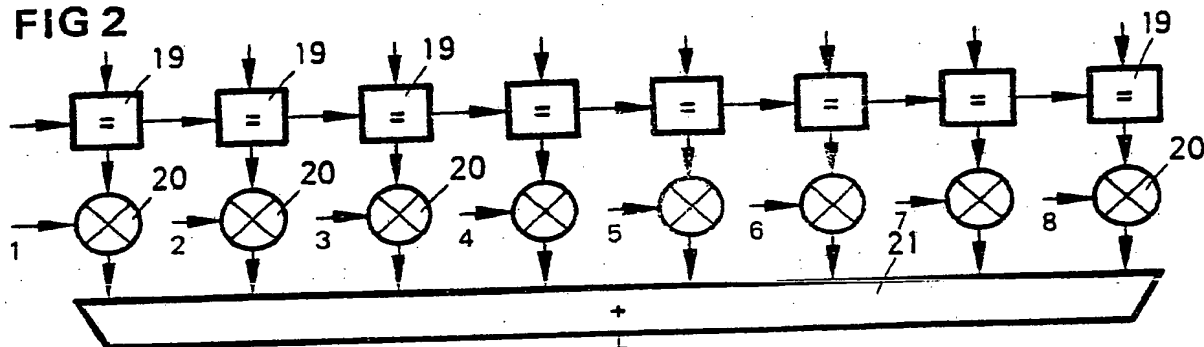
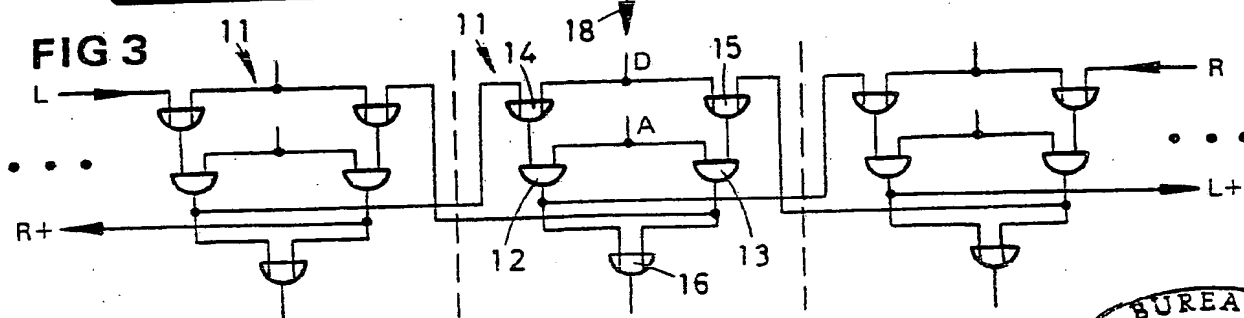
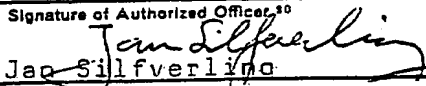
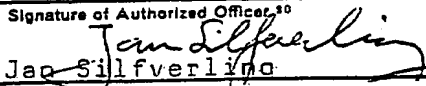
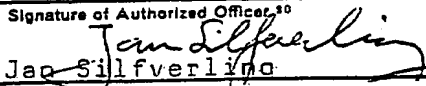


FIG 3



INTERNATIONAL SEARCH REPORT

International Application No PCT/SE84/00083

I. CLASSIFICATION OF SUBJECT MATTER (If several classification symbols apply, indicate all) ¹ According to International Patent Classification (IPC) or to both National Classification and IPC ³ <p style="text-align: center;">H 04 N 1/41</p>								
II. FIELDS SEARCHED <p style="text-align: center;">Minimum Documentation Searched ⁴</p> <table border="1"> <thead> <tr> <th>Classification System</th> <th>Classification Symbols</th> </tr> </thead> <tbody> <tr> <td>IPC 3</td> <td>H 04 N 3/12, 14, 15, 1/38, 40, 41</td> </tr> <tr> <td>US C1</td> <td>358:133, 135, 136, 160, 165, 260</td> </tr> </tbody> </table> <p style="text-align: center;">Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched ⁵</p> <p>SE, NO, DK, FI classes as above</p>			Classification System	Classification Symbols	IPC 3	H 04 N 3/12, 14, 15, 1/38, 40, 41	US C1	358:133, 135, 136, 160, 165, 260
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US C1	358:133, 135, 136, 160, 165, 260							
III. DOCUMENTS CONSIDERED TO BE RELEVANT ¹⁴ <table border="1"> <thead> <tr> <th>Category ⁶</th> <th>Citation of Document, ¹⁶ with indication, where appropriate, of the relevant passages ¹⁷</th> <th>Relevant to Claim No. ¹⁸</th> </tr> </thead> <tbody> <tr> <td> </td> <td> </td> <td> </td> </tr> </tbody> </table>			Category ⁶	Citation of Document, ¹⁶ with indication, where appropriate, of the relevant passages ¹⁷	Relevant to Claim No. ¹⁸			
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<p>⁶ Special categories of cited documents: ¹⁶</p> <p>"A" document defining the general state of the art which is not considered to be of particular relevance</p> <p>"E" earlier document but published on or after the international filing date</p> <p>"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)</p> <p>"O" document referring to an oral disclosure, use, exhibition or other means</p> <p>"P" document published prior to the international filing date but later than the priority date claimed</p> <p>"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</p> <p>"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step</p> <p>"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.</p> <p>"&" document member of the same patent family</p>								
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